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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,953	12/09/2003	Jason Nathaniel Dale	AUS920030582US1	3694

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,953	DALE ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,15,16,24-27 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,8-11,15;16,24-27 and 32-34* is/are rejected.

7)☒ Claim(s) *2-4,6,7,11,16 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 4/12/2006.

2. Claims 1, 3-11, 15-16, 24-27 have been amended.

3. Claims 12-14, 17-23, 28-31 have been cancelled.

4. Claims 32-34 have been added.

5. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Objections

6. Claim 3, 4, 6-7, 11, 16, 25 objected to because of the following informalities:

a. Regarding claims 3, 11, 16, 25, the phrase, "an integer multiple of 2 times the base page size," may cause some minor confusion. As any multiple of 2 will be an integer, it might be simpler just to say, "a multiple of 2, times the base page size."

b. Line 3 of claim 4 should read, "...the same state bits ***and*** share the..."

c. . The last line of claim 6 contains, "whether the an effective address" this should read, "whether an effective address".

d. Claim 7 is objected to because of its dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 6-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

9. With respect to claim 6, the specification does not explicitly support wherein the remaining one of the *m*+1 PSI fields is used to store a value that specifies whether an effective address stored in the same entry needs translation.

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claims 26-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

12. Claims 26-27 are directed towards "a computer program product for translating a received effective address to a real address, comprising: computer program code" but do not claim any form of the software in a tangible computer readable medium, and therefore merely represent abstract idea(s) which taken together fail to accomplish a practical application. Since the claimed software limitations have not been tangibly

embodied (or stored) in a computer readable medium, the software limitation are not capable of being executed by a processor to perform the steps of the claimed limitations because software per se isn't capable of being implemented or executed without a form of tangible embodiment. As such, they fail to produce a useful, concrete and tangible result.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1, 3, 5, 8-11, 15-16 rejected under 35 U.S.C. 102(b) as being anticipated by Kalyanasundharam, U.S. Patent Application Publication 2002/0133685.

14. With respect to claim 1, Kalyanasundharam teaches of a method of storing an effective address (EA) in an effective to real address translation (ERAT) table supporting multiple page sizes including a base page size, wherein the ERAT table comprises a plurality of entries (fig. 2, 3; item 200), the method comprising the steps of: adding a plurality of page size indicator (PSI) fields, to each entry of the ERAT table (figs. 2, 3; paragraph 0015, 0019; where for N different page sizes, there are N-1 size-field bits in each entry in the RAM of the TLB);

wherein the PSI fields of each entry are used to store values that collectively specify either: (i) one of the supported page sizes (fig. 3; paragraph 0045; where each combination of the size bits represents a different page size), or (ii) that an effective address stored in the same entry of the ERAT table does not need translation, and wherein at least one combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation;

storing the EA in one of the entries of the ERAT table (fig. 2; paragraph 0015, 0037; an entry in the virtual address tag entry in the CAM corresponds to the physical address entry in the page table array, RAM, and the overall entry (CAM entry and page table entry) includes the size and the virtual and physical addresses. It is abundantly clear to one of ordinary skill in the art that only one entry in the CAM and page table array corresponds to a specific virtual address (EA). As the entries are located within the CAM and page table entry array, they must have been stored there); and

setting the values of the PSI fields of the one of the entries of the ERAT table to specify either: (i) a page size of the EA, wherein the page size of the EA is one of the supported page sizes (figs. 3A-C; paragraph 0039-0041; where the value of the size bits (PSI fields) in each entry are set in the table in fig. 3A to indicate the corresponding page size), or (ii) that the EA does not need translation.

15. With respect to claim 3, Kalyanasundharam teaches of wherein the supported page sizes include the base page size and at least one other page size that is an integer multiple of 2 times the base page size (fig. 3; the base page size is 8 Kb. The next larger page size is 64 Kb, which is equal to 8 (base page size) times 8 (multiple of 2), all of which are integers).

16. With respect to claim 5, Kalyanasundharam teaches of wherein each added PSI field is configured to store one binary digit (fig. 3; in fig. 3a SZ [2:0] comprises three PSI fields, shown in various locations in the entries in fig. 3b-c. Each field is one bit (a binary digit)).

17. With respect to claim 8, Kalyanasundharam teaches of wherein the effective address (EA) stored in the ERAT table is used to translate another effective address to a real address (fig. 2; paragraph 0015; where the TLB (ERAT table) translates virtual addresses (EA) into physical addresses (RA) using the virtual addresses within).

18. With respect to claim 9, Kalyanasundharam teaches of a method for translating an effective address to a real address, comprising: providing an effective to real address translation (ERAT) table having a plurality of entries each configured to store an effective address (fig. 2; paragraph 0015), a real address corresponding to the stored effective address (fig. 2-3; item 304, 302; paragraph 0015), and

a plurality of page size indicator (PSI) values that collectively specify either: (i) a page size of an effective address stored in the same entry of the ERAT table, wherein the page size of the effective address is one of a plurality of supported page sizes including a base page size (fig. 3; paragraph 0045; where each combination of the size bits represents a different page size, the base page size being 8 Kb), or (ii) that an effective address stored in the same entry of the ERAT table does not need translation, wherein at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation;

receiving the effective address to be translated (paragraph 0007, claim 1);

determining whether the received effective address requires translation (paragraph 0020); and

in the event the received effective address does not require translation, outputting the received effective address as the real address (paragraph 0020).

19. With respect to claim 10, Kalyanasundharam teaches of in the event the effective address requires translation: comparing each of a plurality of ranges of the received effective address to a corresponding range of an effective address stored in each entry of the ERAT table dependent upon the PSI values (fig. 8-9; paragraph 0056),

wherein the received effective address is divided into the plurality of ranges dependent upon a number of the supported page sizes (fig. 2, 8-9; paragraph 0055-0056);

in the event that each range of the received effective address matches the corresponding range of an effective address stored in a particular entry of the ERAT table dependent upon the PSI values: selecting ranges of the real address stored in the particular entry of the ERAT table dependent upon the PSI values (fig. 2; paragraph 0045, 0048); and

outputting the real address, wherein the real address includes the selected, ranges of the real address stored in the particular entry of the ERAT table (fig. 2, 7; paragraphs 0052-0053; when translation is not bypassed, the physical address is selected and outputted).

20. With respect to claim 11, Kalyanasundharam teaches of the limitations as cited above with respect to claim 3.

21. With respect to claim 15, Kalyanasundharam teaches of an apparatus for translating an effective address to a real address, comprising: means for storing an effective to real address translation (ERAT) table (fig. 2; item 200) having a plurality of entries each configured to store an effective address (fig. 2; paragraph 0015), a real

address corresponding to the stored effective address (fig. 2-3; item 304, 302; paragraph 0015), and

a plurality of page size indicator (PSI) values that collectively specify either: (i) a page size of an effective address stored in the same entry of the ERAT table, wherein the page size of the effective address is one of a plurality of supported page sizes (fig. 3; paragraph 0045; where each combination of the size bits represents a different page size, the base page size being 8 Kb), or (ii) that an effective address stored in the same, entry of the ERAT table does not need translation, wherein at least one combination, of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation;

means for receiving the effective address to be translated (fig. 2; paragraph 0007, claim 1; the circuit shown at the top left of the figure receives the VA into the TLB);

means for determining whether the received effective address requires translation (fig. 2; item 207', 207; paragraph 0020); and

means for, in the event the received effective address does not require translation, outputting the received effective address as the real address (fig. 2; item 207; paragraph 0020);

means for, in the event the effective address requires translation, comparing each of a plurality of ranges of the received effective address to a corresponding range of an effective address stored in each entry of the ERAT table dependent upon the PSI values (fig. 2, 8-9; item 202; paragraph 0045, 0048, 0055-0056),

wherein the received effective address is divided into the plurality of ranges dependent upon a number of the supported page sizes (fig. 2, 8-9; paragraph 0055-0056);

means for, in the event the effective address requires translation and each range of the received effective address matches a corresponding range of an effective address stored in a particular entry of the ERAT table dependent upon the PSI values: selecting ranges of the real address stored in the particular entry of the ERAT table dependent upon the PSI values (fig. 2; paragraph 0045, 0048); and

outputting the real address, wherein the real address includes the selected ranges of the real address stored in the particular entry of the ERAT table (fig. 2, 7; paragraphs 0052-0053; when translation is not bypassed, the physical address is selected and outputted).

22. With respect to claim 16, Kalyanasundharam teaches of the limitations as cited above with respect to claim 3.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

25. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

26. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam andLomax, JR. et al., US patent application 2003/0204702.

27. With respect to claims 24 and 26, Kalyanasundharam teaches of all the limitations cited previously with respect to the independent claims (claims 1, 9, and 15). Lomax teaches of implementing a machine-readable medium containing software instructions (paragraph 0017).

It would have been obvious to one of ordinary skill in the art having the teachings of Kalyanasundharam and Lomax at the time of the invention to implement the invention

of Kalyanasundharam as software instructions on a computer readable medium. Their motivation would have been to allow for upgrades and changes to be implemented without changing the hardware, in addition to the advantages of portability of the computer readable medium.

28. With respect to claim 25, Kalyanasundharam teaches of the limitations as cited above with respect to claim 3.

29. With respect to claim 27, Kalyanasundharam teaches of the limitations cited above with respect to claims 10 and 15.

30. Claims 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Chopra et al., US patent application publication 2002/0156962.

31. With respect to claim 32, Kalyanasundharam teaches of a method for selectively storing an effective address (EA) in an effective to real address translation (ERAT) table supporting multiple page sizes including a base page size, wherein the ERAT table comprises a plurality of entries (fig. 2, 3; item 200), the method comprising the steps of: adding a plurality of page size indicator (PSI) fields to each entry of the ERAT table (figs. 2, 3; paragraph 0015, 0019; where for N different page sizes, there are N-1 size-field bits in each entry in the RAM of the TLB),

wherein the PSI fields of each entry are used to store values that collectively specify one of the supported page sizes (fig. 3; paragraph 0045; where each combination of the size bits represents a different page size);

storing the EA in one of the entries of the ERAT table (fig. 2; paragraph 0015, 0037; an entry in the virtual address tag entry in the CAM corresponds to the physical

address entry in the page table array, RAM, and the overall entry (CAM entry and page table entry) includes the size and the virtual and physical addresses. It is abundantly clear to one of ordinary skill in the art that only one entry in the CAM and page table array corresponds to a specific virtual address (EA). As the entries are located within the CAM and page table entry array, they must have been stored there); and

setting the values of the PSI fields of the one of the entries of the ERAT table to specify a page size of the EA, wherein the page size of the EA is one of the supported page sizes (figs. 3A-C; paragraph 0039-0041; where the value of the size bits (PSI fields) in each entry are set in the table in fig. 3A to indicate the corresponding page size).

Kalyanasundharam fails to explicitly teach of performing the above steps only if the EA requires translation. However, Chopra teaches of enabling and disabling the MMU, and when the MMU is disabled, the EA is used as the physical address, without translation (paragraph 0051-0053).

It would have been obvious to one of ordinary skill in the art having the teachings of Kalyanasundharam and Chopra at the time of the invention to enable/disable the PTE array and CAM of Kalyanasundharam based on the translation bypass signal as taught in Chopra. Their motivation would have been to reduce power consumption of the device by not using power to process matches in the TLB when they are going to be ignored in the end result. As the CAM and PTE array are not accessed in the combination, the above steps can only executed when translation is required.

32. With respect to claim 33, Kalyanasundharam teaches of wherein a translation disabled (TD) indicator provided with the EA determines if the EA requires translation (fig. 2, 7; paragraph 0020, 0052; it is abundantly clear to one of ordinary skill in the art that the translation bypass signal must be provided with the EA. If it was provided before the EA is provided, the result of the prior translation operation could result in an invalid result. If provided after the EA is provided, it could result in the TLB not knowing that translation is to be bypassed, and outputting a translated result that is not correct).

33. With respect to claim 34, Kalyanasundharam teaches of wherein a PSI field is added to each entry of the ERAT table for each supported page size except for the base page size (fig. 3; paragraph 0015, 0019; since when N different page sizes are supported, N-1 size field bits are used, if only the base size is supported, there would be no size fields used, thus there isn't one for the base page size).

Allowable Subject Matter

34. The indicated allowability of claims 3-4, 7, 9, 11, 26 are withdrawn in view of the extensive amendments to the respective claims. Rejections based on prior art are above.

35. Claims 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

36. Claims 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the above objection and if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

37. Applicant's arguments filed 4/12/2006 have been fully considered but they are not persuasive.

38. The applicant argues with respect to claims 1-11, 15-16, 24-27, specifically independent claims 1, 9, 15, 24, 26 that Kalyanasundharam fails to teach of:

> ***PSI fields that collectively specify either:***
>
> ***(i) a page size of the EA stored in the same entry of the ERAT table, wherein the page size of the EA is one of the supported page sizes including a base page size, or***
>
> ***(ii) that the EA stored in the same entry of the ERAT table does not need translation, and wherein at least one of the combination of the values of the PSI fields of each entry specifies tha the effective address stored in the same entry does not need translation***

The examiner disagrees. Figures 3a-c, clearly teaches of (i) as the SZ bits located in each entry (figs 3b-c), when combined with the other SZ bits in that entry indicate the page size of that entry shown in fig. 3a. When all of the SZ bits are 0, the base page size of 8 Kb is indicated. As Kalyanasundharam teaches this, it meets these

limitations because they are claimed in the alternative, either (i) or (ii), as opposed to being claimed (i) and (ii).

39. Applicant's arguments directed to claims 2, 4, and 6-7 fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

41. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

42. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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